

COMPACTA UNIBOARD

USER'S MANUAL

VERSION 1.0

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## 1.0 INTRODUCTION

The COMPACTA UNIBOARD is a compact, highly versatile single-board microcomputer designed to fill the need for a low cost, yet highly functional computing system. An optimal mix of ROM, RAM, and I/O resources gives the UNIBOARD the power to run today's most sophisticated 8-bit operating systems. Through very generous use of Large Scale Integration the UNIBOARD provides the user with the following features:

- o Motorola 6809E microprocessor
- o 64K bytes of DRAM
- o 4K bytes of ROM or EPROM
- o Single/Double density, 5 $\frac{1}{8}$ " Floppy Disk controller
- o DMA channel on the Floppy Disk controller
- o Video display control with programmable formats
- o Parallel keyboard interface
- o Parallel (CENTRONICS compatible) printer interface
- o Dual timer for Real Time Clock and time measurements
- o Serial Interface with 20 ma, and RS232C
- o Expansion interface with DMA channel

## 2.0 FUNCTIONAL DESCRIPTION

For descriptive purposes, the circuitry on the UNIBOARD can be divided into ten functional blocks:

- 1) Timing and Control logic
- 2) Microprocessing Unit (MPU)
- 3) Random Access Memory (RAM)
- 4) Read Only Memory (ROM/PROM)
- 5) Floppy Disk Interface
- 6) Parallel Interface
- 7) Serial Interface
- 8) Video Display
- 9) Direct Memory Access Controller (DMAC)
- 10) Expansion Interface

as shown in the block diagram in appendix A.

### 2.1 TIMING AND CONTROL LOGIC

Timing for the UNIBOARD is derived from a single 32,000 Mhz crystal. Part of the inverter U-17 is connected as an oscillator which is buffered and then fed to a divider chain. This divider chain produces a 16 Mhz signal which is used for video dot timing, and a 1 Mhz signal which is used as the main system E clock. The divider also produces signals that clock a section of U-27 to produce the Q clock for the 6809E CPU.

The UNIBOARD owes its simplicity to the ability to interleave CPU cycles with Video Display cycles. The CPU accesses memory during the positive portion of its E clock and



the video display is allowed to access the RAM during the negative or low portion of this clock. To allow the high video character rates required for 80 or more characters per line, the RAM is accessed by the CRTC two bytes at a time. The RAM can thus be considered 8 bits wide for the CPU and 16 bits wide for the CRTC.

U-34, a quad D-type flip-flop is connected as a recirculating shift register which divides each half of the system clock (1 mhz) into eight discrete states. This state machine establishes precise timing from which all control signals for the RAM memory array and the video display section are derived. Since the CRTC scans the video memory sequentially, all row addresses are provided to the RAM in less than 2 Ms thus satisfying the RAM refresh requirements. The CRTC chip must be properly programmed prior to RAM usage.

Address space decoding is performed by a Programmable Array Logic (PAL) device. This PAL decodes the required chip select strobes for the different peripherals on the CPU address space. Appendix B lists these addresses. Further decoding of the I/O space is done by a section of U-26, a 2-to-4 line decoder. A second PAL, U-40, is responsible for derivation of the Column Address Strobes (CAS) for the RAM array. In addition, this PAL generates the enabling signals for the two RAM bidirectional buffers and the Read (FDCRD) and Write (FDCWR) strobes for the Floppy Disk Controller.

## 2.1 MICROPROCESSING UNIT (MPU)

The 6809E Microprocessor is the heart of the UNIBOARD. This MPU performs all system processing functions and generates all the address and control signals to access memory and I/O devices. The two clocks required by the MPU are derived from the timing and control section previously described. These clocks, E and Q, are gated by sections of NAND gate U-20. These clocks are stopped when control of the bus is given to the DMAC during DMA transfers. Synchronization of the DMA cycles is done by flip-flop U-21. The E clock on the MPU is pulled up to Vcc to satisfy its input level requirement.

There are three bus structures in the 6809E MPU. The first bus is the Data bus over which 8 bits of information are transferred between the MPU and other devices such as the ROM or the I/O. The second bus is the 16 bit address bus which holds the address of the device being "talked to" or "heard from" by the MPU. A third bus structure contains a signal to control the direction of transfers across the Data bus (R/W), the enabling clock E, the re-start signal RESET and the interrupt request signal IRQ. The other interrupt request signals, FIRQ and NMI, are not used in the UNIBOARD.

## 2.3 RANDOM ACCESS MEMORY (RAM)



The RAM is implemented with four banks of 16K-by-1 dynamic memory chips. These memory devices have multiplexed addresses and require precise address strobing clocks. The MPU addresses are multiplexed by U-31 and U-39 and supplied to the RAM during the positive portion of E. The CRTC addresses are multiplexed by U-35 and U-43 and supplied to the RAM during the negative or low portion of E. In each of these halves of the E clock, the multiplexer set is switched to supply the Row Address during the early part of the cycle and the Column Address during the latter part of the cycle. The signals to strobe these addresses, RAS and CAS, are derived from the state machine U-34.

The four memory banks are organized into two odd address and two even address blocks. The odd blocks are accessed by the MPU when A0 is a logic one. The even blocks are accessed by the MPU when A0 is high. Both odd and even banks are accessed by the CRTC simultaneously during the low portion of the E clock. Data for the CRT display section are latched by U-57 and U-58 during the rising edge of E. Buffers U-36 and U-44 interface the RAM data lines to the MPU data bus. Enable signals for these buffers are derived by U-40. U-36 is enabled during odd addresses while U-44 is enabled during even addresses.

### 2.4 READ ONLY MEMORY (ROM/EPROM)

This section provides the user with up to 4K bytes of EPROM or ROM that can be installed in U-14. This socket can accommodate a 2732 or 2716 EPROM and any pin compatible ROM. The required chip select for this device is derived by the memory decoding PAL. The output of the ROM/EPROM is enabled only during the positive (high) portion of E during MPU read cycles.

### 2.5 FLOPPY DISK INTERFACE

Up to four 5-1/4" and four 8" floppy disks drives can be controlled simultaneously by the UNIBOARD. Any mixture of sizes and densities can be handled under software control. The Floppy Disk Controller interfaces directly to the memory during floppy disk transfers by means of a DMA channel. Commands and data transfers between the MPU and the CRTC occur through the bi-directional data bus.

The auxiliary floppy control circuit U-51 performs data separation during disk reads and data pre-compensation during disk writes. The PLL data separator requires an external VCO implemented by U-46. Timing for the write pre-compensation is done by U-45.

Interface to the floppy drive is done via schmitt-trigger buffers in U-29 which provide noise immunity to signals coming from the drive. Open-collector buffers interface all signals going to the drive.

### 2.6 PARALLEL INTERFACES



A 6522 Versatile Interface Adapter (VIA) provides the UNIBOARD with interfaces to a CENTRONICS compatible printer and to a parallel ASCII keyboard. The VIA also includes two user programmable timer/counters that have 16 bit resolution. These timer/counters can be used for real time measurement and control.

The parallel keyboard is interfaced on the A side of the VIA. The data available strobe is attached to control input CA1. This input can be programmed for interrupt or polled operation for either positive or negative active strobes. The port can also be programmed for latched or unlatched operation. The keyboard used must be capable of driving one TTL load.

The printer interface utilizes the B side of the VIA. Control output CB2 is used as a data available strobe that can be programmed as a pulse output or as a level output which is reset by CB1. Control input CB1 is the data taken input and can be programmed to reset CB2. CB1 can be programmed for polled or interrupt driven operation.

## 2.7 SERIAL INTERFACE

Using a 6551 asynchronous communications interface adapter (ACIA) the serial interface provides a bi-directional serial data communications channel between the UNIBOARD and peripherals such as terminals, modems and printers. An on-chip baud rate generator allows 15 software programmable baud rates from a standard 1.8432 Mhz crystal. The ACIA also has programmable word lengths, number of stop bits, and parity bit generation and detection.

Level conversion to and from RS232C levels is done by U-4 and U-5. 20 MA current loop interface is also provided. Active or passive current loop is selected by means of jumper block P-6. Selection of 20 MA or RS232C receive channel is done thru jumper block P-7.

## 2.8 VIDEO DISPLAY INTERFACE

The heart of the video display interface is U-28, a 6845 video display controller. The controller generates the signals necessary to interface a digital system to a raster scan CRT display. To display characters on the CRT screen the frames must be continually repeated at a rate faster than the human eye can sample. The data to be displayed is stored in the RAM by the MPU and accessed by the CRT display during the low portion of E. A character generator ROM (U-59) derives the dot patterns which are then converted to serial video by shift register U-75. The character generator includes the complete printable ASCII set as well as some special graphics symbols.

Timing for a hardware cursor and for video reversing is controlled by U-87. Video inversion occurs when the most



significant bit in the character data is a level one.

Two separate interfaces are provided. Composite video is available on connector P-11 after amplification by Q-1. Separate video and sync levels (TTL compatible) are available on connector P-10.

### 2.9 DIRECT MEMORY ACCESS (DMA)

DMA is implemented with a single DMA controller chip, the Motorola 6844 DMAC. Two channels on this chip are decoded and used, one for Floppy Disks transfers and the other for transfers across the external Bus interface. Disk transfers from the on-board FDC take place through MPU cycle-stealing and require no interruption or service by the MPU. This feature allows the UNIBOARD to handle the high data rates of 8" disk drives operating in double density mode. The DMA handshake signals TXRQ1 and ACK1 on the external bus interface permit high speed devices such as COMPACTA's Winchester Disk controller to be readily interfaced.

Once a peripheral requests service through one of the DMA channels, the DMAC stops the MPU clocks and takes over the Address and Control buses. The DMAC also produces a DMA request signal (DRQT) which after being synchronized with E, is used to tri-state the 6809E MPU. The transfer is then completed as a normal memory cycle would with the DMAC supplying the addresses and bus control signals.

### 3.0 SYSTEM INTERFACING

The UNIBOARD with its on-board memory and I/O resources is a complete computer which can be interfaced to numerous external devices such as modems, terminals, printers, and other I/O modules. This section describes the external connections of this single-board computer.

## 3.1 EXPANSION BUS (P1)

This interface includes the MPU address, control and data buses as well as the control signals for channel 1 of the DMA controller. Decoded addresses within the UNIBOARD can be disabled externally by means of the MEMDIS signal. This signal is useful to deny access by on-board peripherals or portions of the RAM or EPROM. The following table fully describes this connector:

PIN	SIGNAL	PIN	SIGNAL
1	n.c.	3	n.c.
2	n.c.	4	n.c.
4	n.c.	5	n.c.
6	n.c.	7	n.c.
8	n.c.	9	n.c.
9	ACK1+ (DMA CH1 ACK)	10	IRQ
11	MEMDIS+ (MEM DISABLE)	12	TXRQ1 (DMA CH1 REQUEST)
13	A15	14	A14
15	A13	16	A12
17	A11	18	A10
19	A9	20	A8
21	A0	22	A1
23	A2	24	A3
25	A4	26	A5
27	A6	28	A7
29	E	30	R/W
31	RESET+	32	D7
33	D6	34	D5
35	D4	36	D3
37	D2	38	D1
39	D0	40	BUSEN+ (DATA BUS ENABLE)

## 3.2 KEYBOARD PORT (P3)

An ASCII encoded keyboard is interfaced through this connector. The interface allows up to 8 data bits and a positive or negative going strobe. The active edge of the strobe is initially defaulted to negative (high to low transition).

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	BIT 7 (MSB)	2	-12 V @ 10 ma.
3	BIT 6	4	RESET IN
5	BIT 5	6	GROUND
7	BIT 4	8	GROUND
9	BIT 3	10	+5 V @ 500 ma.
11	BIT 2	12	+5 V @ 500 ma.
13	BIT 1	14	N.C.
15	BIT 0 (LSB)	16	STROBE

## 3.3 SERIAL PORT (P2)

This port is configured as a Data Communication Equipment (DCE) interface. A null Modem must be used to convert to a Data Terminal Equipment (DTE).

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	PROT. GROUND	2	DATA IN
3	DATA OUT	4	CTS IN
5	RTS OUT	6	DTR OUT
7	SIGNAL GROUND	12	TTY IN (-)
13	TTY OUT (+)	20	DSR/DCD IN
24	TTY IN (+)	25	TTY OUT (-)



## 3.4 8" FLOPPY DISK INTERFACE (P8)

This connector is set up for the SHUGART floppy standard interface. The connector accommodates up to four single/double density, single/double sided drives.

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	GROUND	2	TG43
3	GROUND	4	N.C.
5	GROUND	6	N.C.
7	GROUND	8	N.C.
9	GROUND	10	N.C.
11	GROUND	12	N.C.
13	GROUND	14	SIDE
15	GROUND	16	N.C.
17	GROUND	18	HEAD LOAD
19	GROUND	20	INDEX
21	GROUND	22	N.C.
23	GROUND	24	N.C.
25	GROUND	26	SELECT 0
27	GROUND	28	SELECT 1
29	GROUND	30	SELECT 2
31	GROUND	32	SELECT 3
33	GROUND	34	DIRECTION
35	GROUND	36	STEP
37	GROUND	38	WRITE DATA
39	GROUND	40	WRITE GATE
41	GROUND	42	TRACK 00
43	GROUND	44	WRITE PROTECT
45	GROUND	46	READ DATA
47	GROUND	48	N.C.
49	GROUND	50	N.C.

## 3.5 MINI-FLOPPY DISK INTERFACE (P9)

This connector will accommodate up to four single/double density, single/double sided mini-floppy drives. The SHUGART mini-floppy interface has been adhered to with the exception of SELECT 3 which is not specified in the original SHUGART document.

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	GROUND	2	N.C.
3	GROUND	4	N.C.
5	GROUND	6	SELECT 3
7	GROUND	8	INDEX
9	GROUND	10	SELECT 0
11	GROUND	12	SELECT 1
13	GROUND	14	SELECT 2
15	GROUND	16	MOTOR ON
17	GROUND	18	DIRECTION
19	GROUND	20	STEP
21	GROUND	22	WRITE DATA
23	GROUND	24	WRITE GATE
25	GROUND	26	TRACK 00
27	GROUND	28	WRITE PROTECT
29	GROUND	30	READ DATA
31	GROUND	32	SIDE
33	GROUND	34	N.C.

### 3.6 COMPOSITE VIDEO INTERFACE (P11)

This interface provides more than 2 volts peak to peak into a 75 ohm load. The video signal available on this connector conforms to EIA standard RS-170.

PIN NUMBER	SIGNAL
1	GROUND
2	VIDEO
3	GROUND

### 3.7 SEPARATE VIDEO AND SYNC INTERFACE (P10)

This interface should be used with CRT monitors requiring separate video and sync levels. Better than 2 volts peak are available into 2k ohm loads.

PIN NUMBER	SIGNAL
1	VERTICAL SYNC
2	HORIZONTAL SYNC
3	VIDEO
4	GROUND

### 4.0 POWER REQUIREMENTS

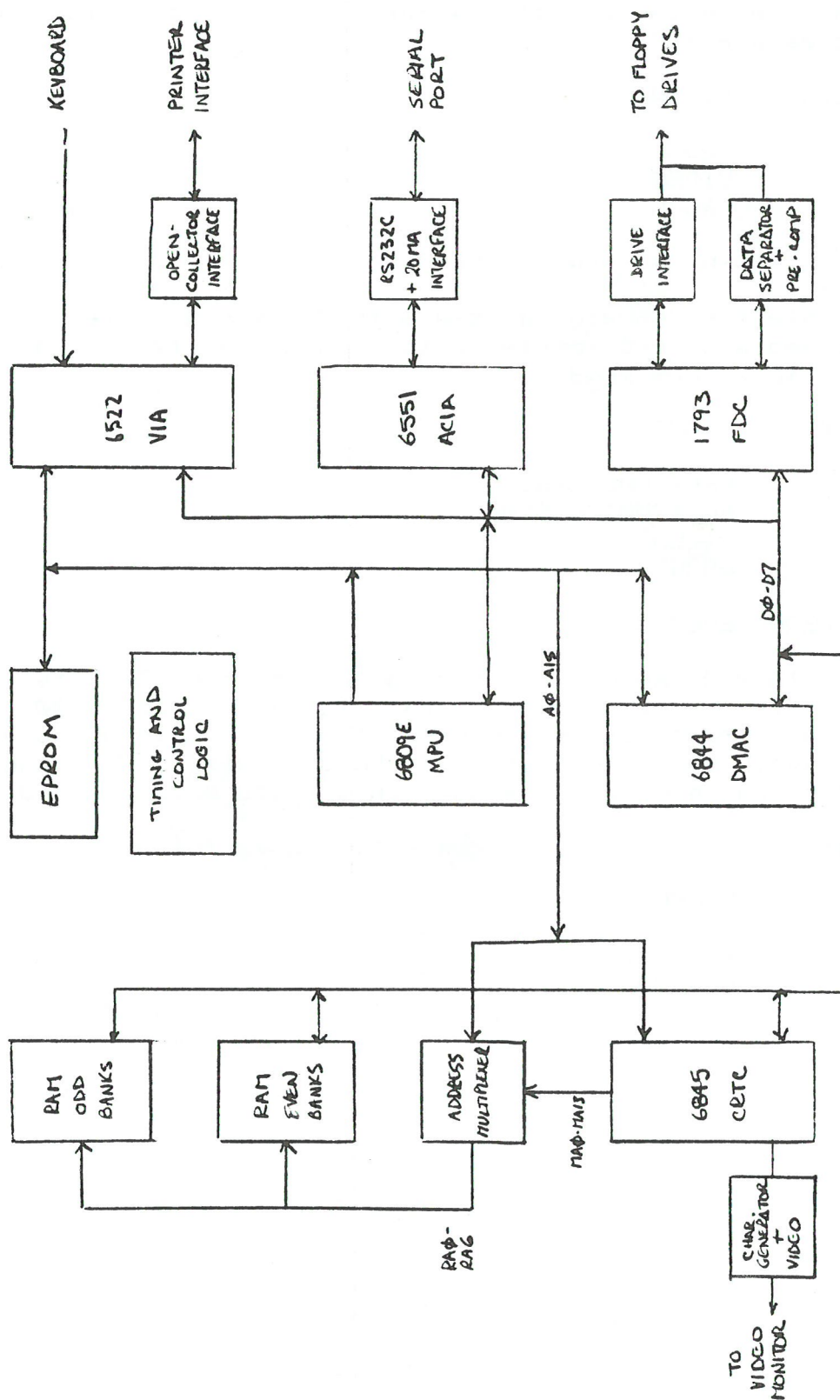
The UNIBOARD when fully populated requires +5 Volts at 1.5 Amps, +12 Volts at 0.75 Amps, and -12 Volts at .100 Amps. Provision was made for an on-board -12 Volts DC-to-DC converter which can supply the required -12 Volt power. U89 and its associated components are used when this feature is desired.

Pinout of the input power connector is as follows:

PIN NUMBER	SIGNAL
1	+5 VOLTS
2	GROUND
3	-12 VOLTS (OUTPUT IF ON-BOARD DC-TO-DC USED)
4	+12 VOLTS



APPENDIX A - BLOCK DIAGRAM



## APPENDIX B - MEMORY MAP

ADDRESS RANGE	DEVICE
0000-DFFF	RANDOM ACCESS MEMORY
E000-EF1F	VIDEO DISPLAY RANDOM ACCESS MEMORY
EF00-EF1F	6844 DMA CONTROLLER
EF20-EF2F	6522 VIA
EF30-EF33	1793 FLOPPY DISK CONTROLLER
EF40-EF43	6551 ACIA
EF44-EF45	6845 CRT CONTROLLER
EF48-EF48	FLOPPY CONTROL LATCH (WRITE ONLY)
EF48-EF48	SENSE SWITCH (READ ONLY, BITS 0-2)

This is the memory map provided with standard versions of the UNIBOARD. Custom PAL's can be provided for different configurations.

APPENDIX C - JUMPERS AND SWITCHES

C.1 P7 - SERIAL RECEIEVE CONFIGURATION

This jumper selects 20 MA. current loop (Jumper 1-2), or RS232C (Jumper 2-3) interface on the serial I/O channel.

C.2 S1 - RESET AND SENSE SWITCH

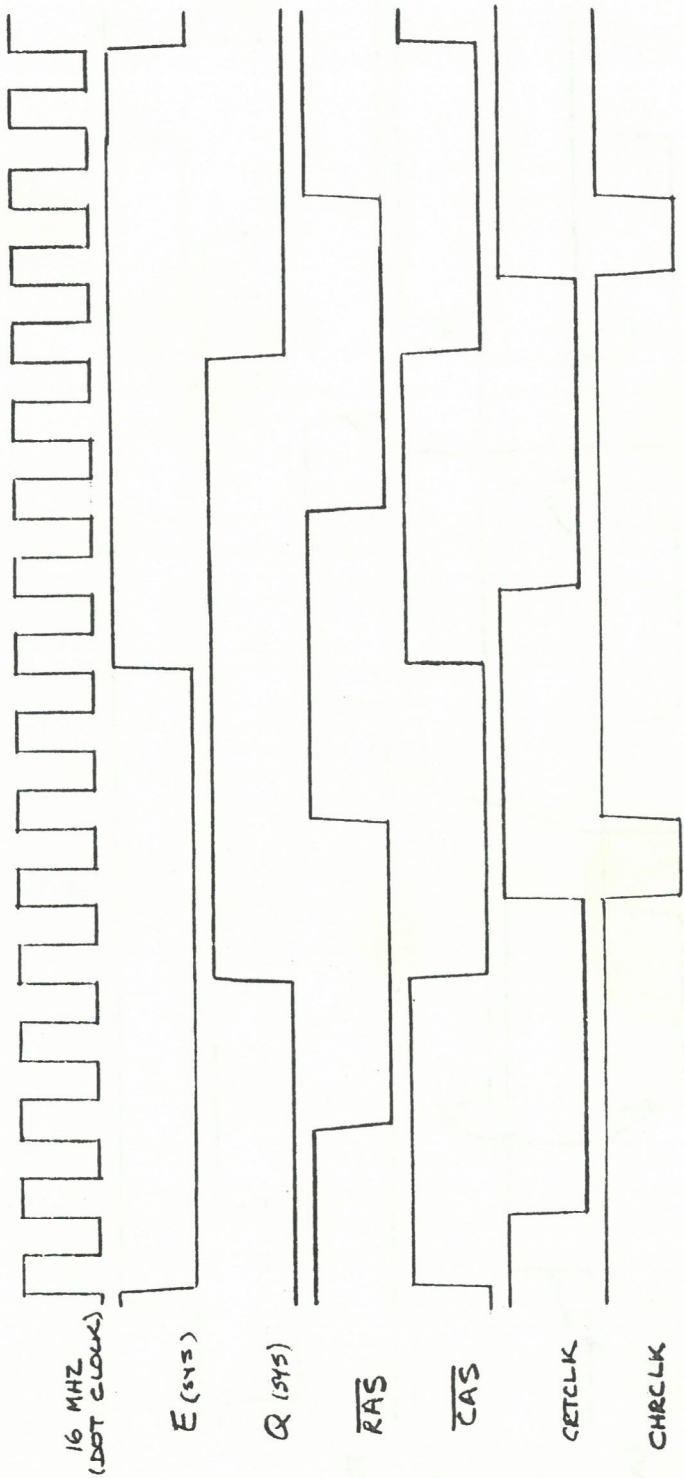
Switch 1 of this multiple switch is the on-board reset. Reset is asserted when the switch is in the 'on' position.

Switches 2-4 correspond to data bits 2, 1, and 0 respectively when read on location EF48. The OS9 serial port driver reads these three bits and loads this code in the baud rate select register in the 6551 ACIA. The default baud rate can later be altered with the TMODE utility.

Switch 4 is read by the OS9 BOOT module to determine the disk size to boot from. For 8" disks, the switch must be in the 'off' position.



APPENDIX D - MAIN TIMING DIAGRAM



APPENDIX E - DMA TIMING DIAGRAM

